



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/993,712

11/27/2001

Toshifumi Nakatani

0819-0702

8353

22204

7590

07/09/2004

NIXON PEABODY, LLP

401 9TH STREET, NW

SUITE 900

WASHINGTON, DC 20004-2128

EXAMINER

WARREN, MATTHEW E

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 07/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/993,712	Applicant(s) NAKATANI ET AL.	
	Examiner Matthew E Warren	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the Amendment filed on March 17, 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 6, 7, 13, 14, 19, 20, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulatti et al. (US 6,153,914) in view of Burr (US 6,137,142).

In re claim 1, Mulatti et al. shows (fig. 7) a high frequency switch circuit device (col. 2, lines 19-27) comprising a semiconductor substrate (7) including a p-type substrate region, and a p-channel type FET (P2) provided in the p-type substrate region and functioning as a high frequency switching element including a source (10), drain (9), a gate (under P2 label) and an n-type well (8). A voltage supply node (Vcc) is connected to the n-type well for supplying a voltage to the well. A high frequency separation means (inductor L2) is provided between the n-type well and the voltage supply node for separating a high frequency component of a signal flowing between the n-type well and the voltage supply node. Mulatti shows all of the elements of the claims except the source electrode connected to the source and separated from an electrode of the n-type well. Burr shows (fig. 3a) a semiconductor device in which a FET is formed in an n-well (311) and has a source (308). The source has an electrode (315)

Art Unit: 2815

and the n-well has a separate contact (318) for providing a bias voltage. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the switching element of Mulatti by providing a separate source electrode as taught by Burr to provide a separate each component with a desired potential.

In re claim 6, Mulatti et al. shows (fig. 7) the circuit device further comprising another high frequency signal separation means (L3) provided between the n-type well and a ground (Gnd on bottom of substrate) so as to separate a high frequency component of a signal flowing between the n-type well and the ground.

In re claim 7, Mulatti et al. shows (fig. 7) that the separation means is an inductor (L2).

In re claim 13, Mulatti et al. shows (fig. 7) a high frequency switch circuit device (col. 2, lines 19-27) comprising a semiconductor substrate (7) including a p-type substrate region, and an n-channel type FET (N2) provided in the p-type substrate region and functioning as a high frequency switching element including a source (12), drain (11), a gate (under N2 label) and an p-type well (130). A barrier layer (N-well 140) is provided between the p-type substrate region and the p-type well and serving as a barrier against a flow of high frequency signal between the p-type substrate region and the p-type well. A high frequency separation means (inductor L4) is provided between the p-type well and a ground (Gnd on top of substrate) for separating a high frequency component of a signal flowing between the p-type well and the ground.

In re claim 14, Mulatti et al. shows (fig. 7) that the barrier layer (N-well 140) is an n-type of well provided between the p-type substrate region and the p-type well. The circuit further comprises a voltage supply node (Vcc) connected to the N-type well for supplying a voltage to the n-type well and another high frequency signal separation means (inductor L21) provided between the n-type well and the voltage supply node. The separation means separates a high frequency component of a signal flowing between the n-type well and the voltage supply node.

In re claim 19, Mulatti et al. shows (fig. 7) the circuit device further comprising another high frequency signal separation means (L3) provided between the p-type well and a ground (Gnd on bottom of substrate) so as to separate a high frequency component of a signal flowing between the p-type well and the ground.

In re claim 20, Mulatti et al. shows (fig. 7) that the separation means is an inductor (L2).

In re claims 26 and 27, Burr shows (fig. 3a) that the semiconductor device further comprises a drain electrode (over 310 and 314) connected to a drain (310 and 303 respectively) and separated from the electrode of the n-well.

Claims 2-5 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulatti et al. (US 6,153,914) in view of Burr (US 6,137,142) as applied to claims 1 and 13 above, and further in view of Maeda et al. (US 6,452,249 B1).

In re claims 2-4, and 15 –17, Mulatti et al. discloses the invention in the form of a bulk silicon semiconductor device but does not show that the device is formed in a SOI

Art Unit: 2815

substrate. Maeda shows (fig. 65) a portion of a high frequency circuit (col. 1, lines 7-17) having an insulative layer (12 and 2) surrounding a well region (51) and extending downward from a surface of the semiconductor substrate to a position deep than the well. The device is an SOI substrate having the well on an insulating layer (2). The SOI device is a silicon substrate having a buried insulative layer made of silicon oxide to isolate the device regions from each other (col. 46, lines 5-20). Maeda discloses (col. 44, lines 50-60) that the semiconductor device is interchangeably applicable to an SOI as well as a bulk substrate. Therefore it would have been common to one of ordinary skill in the art at the time the invention was made to modify the high frequency circuit formed in the bulk substrate of Mulatti and Burr by forming it on SOI substrate because Maeda teaches that bulk devices can also be applied to SOI substrates.

In re claims 5 and 18, a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17**(footnote 3). See also in re Brown, **173 USPQ 685**; In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**; In re Avery, **186 USPQ 116** in re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the

Art Unit: 2815

product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process.” In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

Claims 8 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulatti et al. (US 6,153,914) in view of Burr (US 6,137,142) as applied to claims 1, 7, 13, and 20 above, and further in view of Ghoshal (US 5,952,893).

In re claims 8 and 21, Mulatti et al. discloses the use of an inductor but does not specifically disclose that the inductor is a coil shaped line. It is well known in the art, that inductors can be coil shaped lines. However, Ghoshal discloses (col. 7, lines 8-13) a high frequency circuit in which a typical inductor is formed having a coil shaped line. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the inductor of Mulatti and Burr by forming a coil shaped line because Ghoshal teaches that inductors are well known to have coil shaped lines.

Claims 9, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulatti et al. (US 6,153,914) in view of Burr (US 6,137,142) as applied to claims 1 and 13 above, and further in view of Fujioka et al. (US 6,492,872 B1).

In re claims 9 and 22, Mulatti et al. and Burr shows all of the elements of the claims except the high frequency separation means being a resistor. Fujioka et al. discloses (col. 7, lines 30-44), a resistor used to separate/cut high frequency signal components in a circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the high frequency separation

Art Unit: 2815

means of Mulatti and Burr by using a resistor as taught by Fujioka to separate a high frequency signal component in a circuit.

Claims 10 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulatti et al. (US 6,153,914) in view of Burr (US 6,137,142) and Fujioka et al. (US 6,492,872 B1) as applied to claims 1, 9, 13, and 22 above, and further in view of Sekiya et al. (US 4,433,920).

In re claims 10 and 23, Mulatti et al., Burr, and Fujioka et al. show all of the elements of the claims except the resistor made of polysilicon. It is well known in the art of semiconductors that resistors can be made of polysilicon. However, Sekiya et al. discloses (col. 11, lines 29-34) that resistors used in high frequency divider circuits comprise polysilicon. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the resistor of Mulatti, Burr, and Fujioka by using polysilicon because Sekiya teaches that polysilicon is suitable material for resistors used in semiconductor devices.

Claims 11, 12, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mulatti et al. (US 6,153,914) in view of Burr (US 6,137,142) as applied to claims 1 and 13 above, and further in view of Griffin et al. (US 6,236,070 B1).

In re claims 11, 12, 24, and 25 Mulatti et al., Burr, and Fujioka et al. show all of the elements of the claims except the high frequency separation means being a transmission line. Griffin et al. discloses (col. 7, line 55 - col. 8, line 6) a frequency

Art Unit: 2815

divider (separation means) being a transmission line having $\frac{1}{4}$ wavelength sections of length (see also fig. 13). Griffin does not disclose that the line length is an odd number multiple of the $\frac{1}{4}$ of a wavelength, however Griffin does suggest that the line can be any desired length (col. 8, lines 1-6). Thus, it would have been an obvious to form the transmission line having the desired line length since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the high frequency separation means of Mulatti and Burr by using a transmission line having the desired length as taught by Griffin to divide a signal into desired components.

Response to Arguments

Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

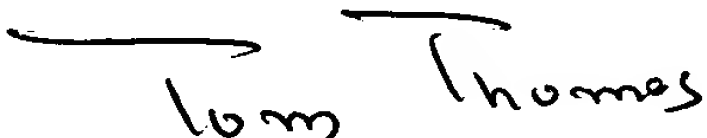
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW

June 20, 2004


TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800